APPENDIX C

complete set of "clean" claims

pursuant to 37 C.F.R. §1.121(c)(3)

1. A semiconductor device comprising, in combination, a silicon substrate having a first and second surface; a first layer disposed on said first surface and having impurities of the n or p conductivity type uniformly distributed throughout the volume of said first layer; a second layer disposed on said first layer; said second layer having impurities of the same type as those in said first layer uniformly distributed therethrough and having a substantially uniform resistivity; the concentration of impurities in said second layer being greater than the concentration of impurities in said first layer; and a plurality of diffusions of a conductivity type opposite to that of said second layer uniformly distributed into the surface of said second layer and defining p-n junctions therein; said plurality of diffusions being separated by invertible channels in said second layer.

2. The device of claim 1 wherein the resistivity of said second layer is lower than that of said first layer.

3. The device of claim 1 wherein the thickness of said first layer is greater than that of said second layer.

4. The device of claim 2 wherein the thickness of said first layer is greater than that of said second layer.

5. The device of claim 1 wherein said device has a given blocking voltage; and wherein the total thickness of said first and second layers is less than the thickness of a single layer of epitaxial silicon designed to block the given blocking voltage.

6. The device of claim 2 wherein said device has a given blocking voltage; and wherein the total thickness of said first and second layers is less than the thickness of a single layer of epitaxial silicon designed to block said given blocking voltage.

7. The device of claim 3 wherein said device has a given blocking voltage; and wherein the total thickness of said first and second layers is less than the thickness of a single layer of epitaxial silicon designed to block said given blocking voltage.

8. The device of claim 4 wherein said device has a given blocking voltage; and wherein the total thickness of said first and second layers is less than the thickness of a single layer of epitaxial silicon designed to block said given blocking voltage.

9. The device of claim 8 wherein said device is a vertical conduction power MOSFET.